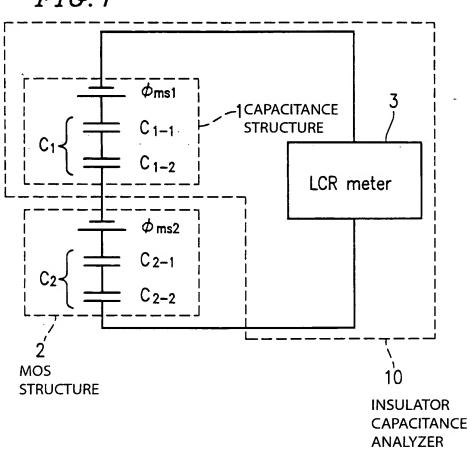
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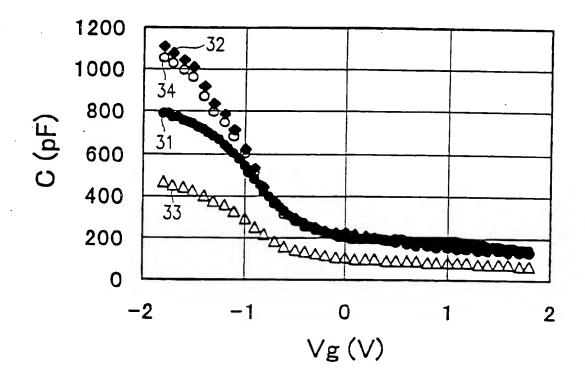
$$FIG.2 \\ C_{1} \left\{ \begin{array}{c} \downarrow \\ \downarrow \\ \downarrow \\ C_{1-1} \\ \downarrow \\ \downarrow \\ C_{2-1} \\ \downarrow \\ C_{2-2} \end{array} \right\} 1 \\ C_{2} \left\{ \begin{array}{c} \downarrow \\ \downarrow \\ \downarrow \\ \downarrow \\ \downarrow \\ C_{2-2} \\ \downarrow \\ C_{2-2} \end{array} \right\} 2$$

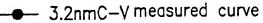
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FIG.3

## NMOS C-V Characteristics





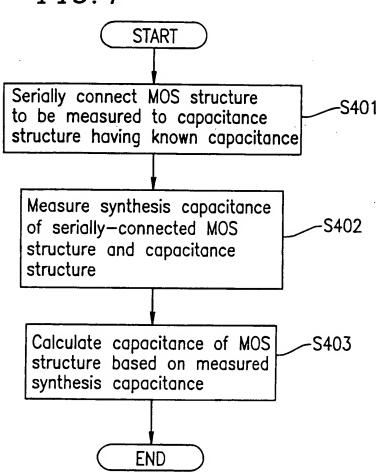
2nmC-V ideal curve

-A— Synthesis curve -O— 2nmC-V conversion curve

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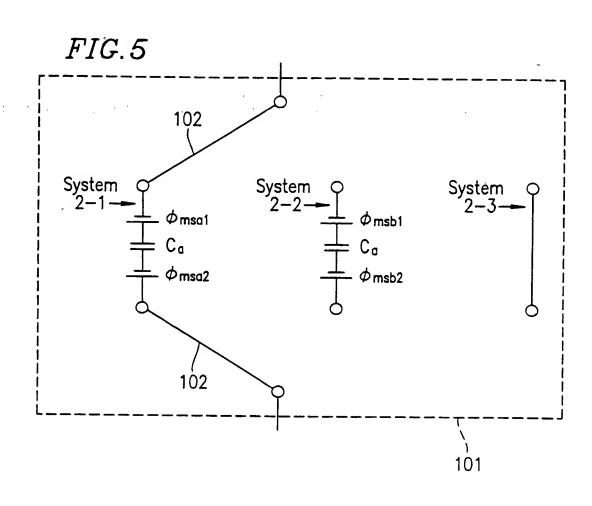


## FIG.4



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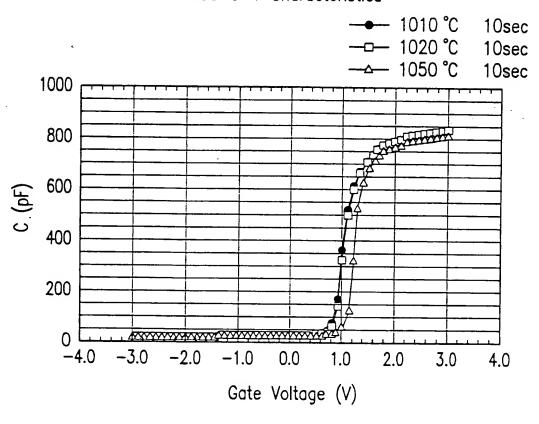


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FIG.6

PMOS C-V Characteristics



Active Area: 9E-4cm<sup>2</sup>

w/o Well Imp. Gate SiON: NO/N2

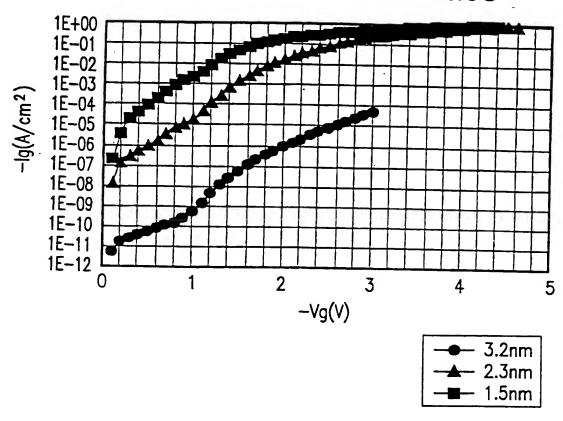
poly Si: 200nm P+lmp.: BF<sub>2</sub>

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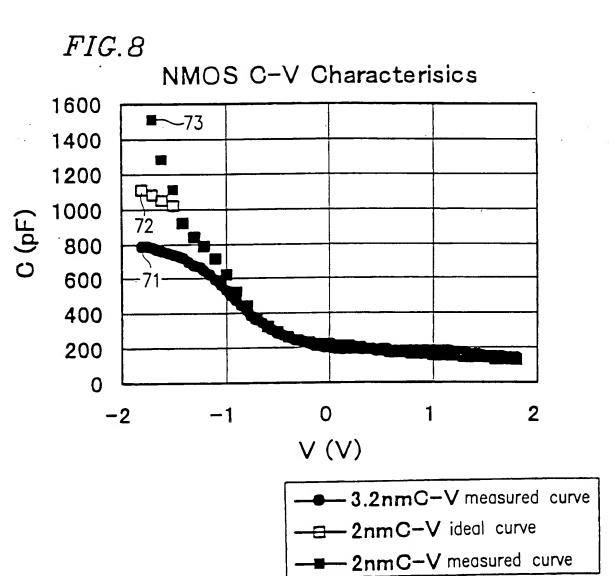
FIG.7

## NMOS I-V Characteristics



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